UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,501	03/12/2004	Dong-Han Kim	9903-075	1864

20575 7590 10/05/2005

MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,501	KIM, DONG-HAN	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/12/04; 4/25/05; 9/21/05-
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 and 2a-2c should be designated by a legend such as --Prior Art-- instead of "Conventional Art" because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6 and 9-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Fukuda (US Pat. No. 6,127,729).

Regarding claims 1 and 11, Fukuda teaches a semiconductor chip comprising:

a plurality of outer edges (consider the corners of chip 3 shown in figs. 2 and 9];

a peripheral area located adjacent to the outer edges (portion of chip 3 that includes pads 7,8 and/or 22) [see figs. 2 and 9]; and

a main circuit area (Internal Circuit A-D) located within the confines of the peripheral area, the main circuit area including integrated circuits [see figs. 2 and 9],

wherein the peripheral area includes chip pads (8) connected to the integrated circuits [see figs. 2 and 9], and also a plurality of test pads (7 and/or 22) electrically connected to the integrated circuits for testing electrical properties of the integrated circuits [see figs. 2 and 9].

In addition, Fukuda teaches a tape wiring substrate (1) [see fig. 1].

Regarding claims 2 and 12, Fukuda further teaches that the chip pads (8) are arranged in rows adjacent the main circuit area of the semiconductor chip, and the test pads (7 and/or 22) are located within the rows of chip pads [see figs. 2 and 9].

Regarding claims 3 and 13, Fukuda further teaches that the chip pads (8) and the test pads (7 and/or 22) are arranged at substantially uniform intervals [see figs. 2 and 9].

Regarding claims 4 and 14, Fukuda further teaches that the test pads (7 and/or 22) are located at the ends of the rows of chip pads (8) [see figs. 2 and 9].

Regarding claims 5 and 15, Fukuda further teaches that the configuration of the main circuit area (Internal Circuit A-D) is arranged to form corners, and the test pads (7 and/or 22) are located near the corners of the main circuit area [see figs. 2 and 9].

Regarding claims 6 and 16, Fukuda further teaches that the chip pads (8) are arranged in rows parallel to at least one set of opposed outer edges of the

semiconductor chip, and the test pads (7 and/or 22) are arranged within the rows of chip pads [see figs. 2 and 9].

Regarding claim 9, the limitation describing how the test pads are formed (e.g. by bump bonding) contains method of process of making characteristics; therefore given no patentable weight in determining patentability of the final device structure. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 10, Fukuda further teaches that the chip comprises one of an edge-pad-type chip and a center-pad-type chip (Internal Circuit A-D) [see figs. 2 and 9].

4. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Aiki et al. (JP 2002-303653).

Regarding claims 1 and 11, Aiki et al. teaches a semiconductor chip comprising:

a plurality of outer edges (consider the corners of chip 1 shown in fig. 1];

a peripheral area (2) located adjacent to the outer edges [see fig. 1]; and

a main circuit area (5) located within the confines of the peripheral area, the main circuit area including integrated circuits [see fig. 1],

wherein the peripheral area includes chip pads (squares without X marks such as 311-313) connected to the integrated circuits [see fig. 1], and also a plurality of test pads (the X marked squares such as 211-213) electrically connected to the integrated circuits for testing electrical properties of the integrated circuits [see fig. 1].

In addition, Aiki et al. teaches a tape wiring substrate (1) [see fig. 1].

Regarding claims 2 and 12, Aiki et al. further teaches that the chip pads (squares without X marks such as 311-313) are arranged in rows adjacent the main circuit area of the semiconductor chip, and the test pads (the X marked squares such as 211-213) are located within the rows of chip pads [see fig. 1].

Regarding claims 3 and 13, Aiki et al. further teaches that the chip pads (squares without X marks such as 311-313) and the test pads (the X marked squares such as 211-213) are arranged at substantially uniform intervals [see fig. 1].

Regarding claims 4 and 14, Aiki et al. further teaches that the test pads (the X marked squares such as 211-213) are located at the ends of the rows of chip pads (squares without X marks such as 311-313) [see fig. 1].

Regarding claims 5 and 15, Aiki et al. further teaches that the configuration of the main circuit area (5) is arranged to form corners (consider the corners of area 5), and the test pads (the X marked squares such as 211-213) are located near the corners of the main circuit area [see fig. 1].

Regarding claims 6 and 16, Aiki et al. further teaches that the chip pads (squares without X marks such as 311-313) are arranged in rows parallel to at least one set of opposed outer edges of the semiconductor chip, and the test pads (the X marked squares such as 211-213) are arranged within the rows of chip pads [see fig. 1].

Regarding claims 7 and 17, Aiki et al. further teaches that the test pads (the X marked squares such as 211-213) are arranged between the rows of chip pads (squares without X marks such as 311-313) [see fig. 1].

Regarding claims 8 and 18, Aiki et al. further teaches that the test pads (the X marked squares such as 211-213) are substantially the same dimensional size as the chip pads (squares without X marks such as 311-313) [see fig. 1].

Regarding claim 9, the limitation describing how the test pads are formed (e.g. by bump bonding) contains method of process of making characteristics; therefore given no patentable weight in determining patentability of the final device structure. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims

or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 10, Aiki et al. further teaches that the chip comprises one of an edge-pad-type chip and a center-pad-type chip (5) [see fig. 1].

Regarding claims 19-20, Aiki et al. further teaches that the tape wiring substrate comprises an insulating base film (1300), wiring patterns (1400) formed on the insulating base film, leads (1511) formed integrally with the wiring patterns, and dummy leads (1520) electrically isolated from the wiring patterns [see fig. 21 (b)].

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

José R. Díaz
Examiner
Art Unit 2815